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Parallel Fabrication of Nanogap Electrodes

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ABSTRACT

We have developed a technique for simultaneously fabricating large numbers of nanogaps in a single processing step using feedback-controlled electromigration. Parallel nanogap formation is achieved by a balanced simultaneous process that uses a novel arrangement of nanoscale shorts between narrow constrictions where the nanogaps form. Because of this balancing, the fabrication of multiple nanoelectrodes is similar to that of a single nanogap junction. The technique should be useful for constructing complex circuits of molecular-scale electronic devices.

The development of a reliable, reproducible fabrication process for nanoscale gaps useful as contact electrodes is one of the major technological challenges faced by molecular electronics. Although a number of approaches have been advanced in recent years,[1−9] to date, there is no viable method to fabricate nanogaps with separations in the sub-5 nm regime by a controlled parallel process as required for production of very large scale integrated molecular circuits.

Recently, a feedback-controlled electromigration (FCE) technique has been developed[2,4,5] and used to controllably create individual nanoscale junctions ranging from few-atom channels to opaque tunnel barriers.[2] This technique differs from earlier electromigration approaches[1] that employed a single voltage ramp, yielding thermal runaway[10] and a random assortment of gap sizes.[1] The salient advantage of FCE is that feedback is used to ensure that nanogap formation occurs through electromigration at a regulated onset temperature in the nanogap region.[2,11,12] The conductance of the resulting nanogap can be controlled to within a factor of 3 of a desired set point, corresponding to control of the electrode separation to better than 1 nm. Until now, formation of multiple nanogaps required that each undergo the FCE process individually, a restriction making FCE too time-consuming for fabrication of complex circuitry.

To overcome this difficulty, we have developed a technique using FCE that permits the simultaneous fabrication of large numbers of nanogaps at room temperature in a single processing step. Our multidevice design naturally balances the power dissipation during the FCE procedure so that all nanogaps undergo electromigration in unison. The essential design feature is that the interjunction resistance is kept lower than the junction resistance, which ensures that none of the individual nanogaps experience thermal runaway.[10] We find that FCE of the parallel combination of nanoelectrodes fabricated in this new geometry behaves similarly to that of single nanogap junctions, with roughly unchanged processing time, and voltage and current levels that scale with the number of nanogaps. As a demonstration, we have used the process to fabricate 16 nanogaps in parallel.

The samples are fabricated using electron beam lithography to construct thick gold leads connected by thin narrow junctions. This makes the resistance of the junction larger than the interjunction resistance, which permits the parallel electromigration of nanogaps. This control of the metallization thickness is achieved through a multiangle shadow evaporation technique (see details in Supporting Information).

Figure 1a shows the time evolution of the conductance−voltage ($G-V$) characteristic of a single thin gold junction during FCE and the resistor model used to analyze these data. The resistor model[2] consists of a lead resistance, R_L, in series with a variable junction resistance, R_n. During FCE of a single junction, a rapid increase in R_n due to electromigration occurs upon reaching a critical level of power dissipation (and a critical temperature[2,12,13]) at the junction. This behavior is characteristic of a junction in the bulk-neck regime where its diameter exceeds 1 nm.[2] In response to an increase in overall resistance, the active feedback loop adjusts V, thereby tracing out the single junction electromigration $G-V$ curve in Figure 1a. The smooth decrease in G over as many as 11 orders of magnitude reflects the controlled electromigration process, where thermal runaway and stochastic breaking of the nanogap are avoided.

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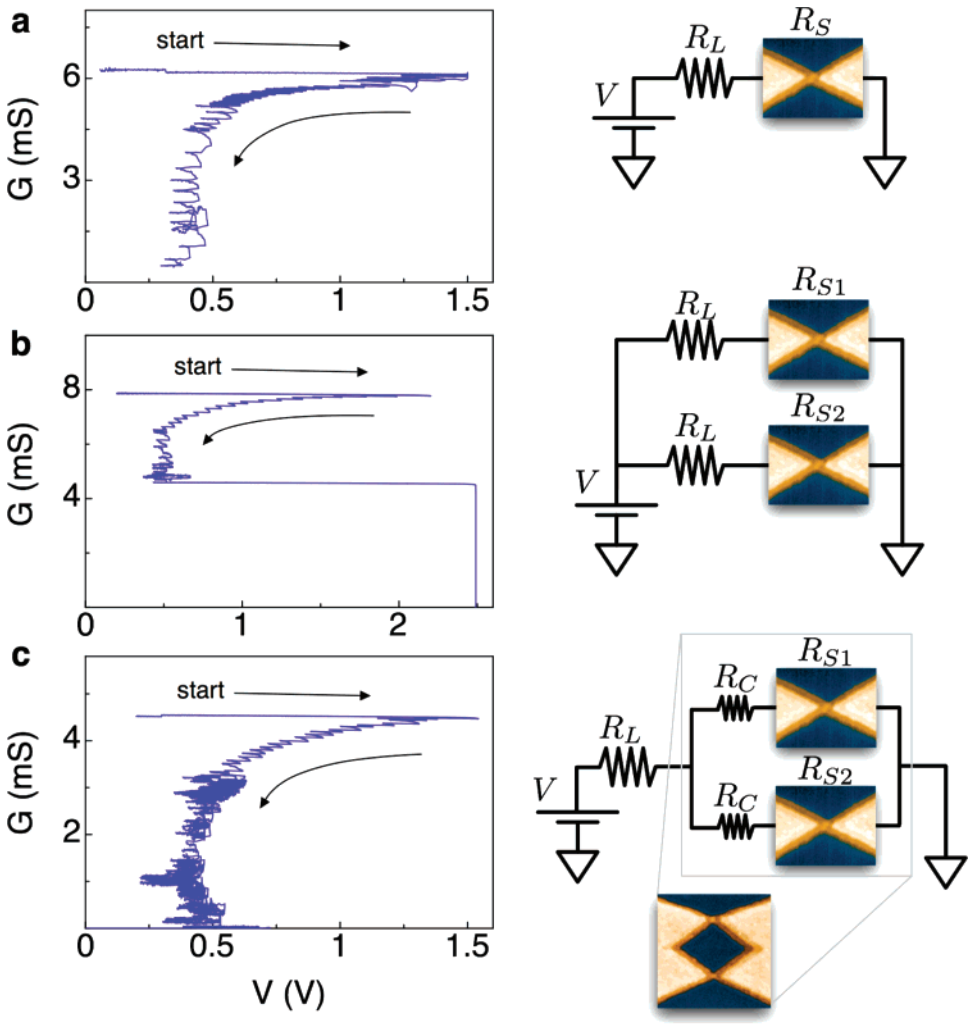

Figure 1. $G-V$ plots measured during FCE of different samples and their equivalent circuit diagrams. (a) FCE of a single junction shows a smooth controllable decrease in G. (b) Two junctions connected by the leads are not able to electromigrate together. Thermal runaway occurs when the second junction breaks discontinuously. (c) Two junctions connected in parallel by low a resistance R_c electromigrate in unison in a parallel process.

If this approach is scaled up by simply connecting two leads together (Figure 1b), we find that FCE consistently fails to make uniform nanogaps in parallel. Instead, gaps form sequentially, as in the $G-V$ curve of Figure 1b. (Sequential gap formation was observed in 4 out of 4 trials.) This behavior is due to the inherent variability of nanolithography. That is, one of the thin junctions (e.g., junction 1 with resistance R_{n1}) will invariably begin to electromigrate at a smaller applied voltage than the other (the junction with resistance R_{n2}). As a result, junction 1 undergoes controlled electromigration until one nanogap is formed, and the resistance of the parallel combination of the two junctions becomes pinned at R_{n2}. At this point, the voltage increases sharply, and the second junction fails in an abrupt, uncontrollable break. Because of the sequential nature of the process, at some point the junction resistances differ by orders of magnitude (junction 1 in the tunnel regime with $R_{S1} \gg h/2e^2 \sim 12$ kΩ, while R_{n2} remains at its initial value near 4 Ω), and simultaneous control over both junctions is impossible. An additional significant problem is that the first nanogap is subjected to a large voltage after it is formed, which can considerably alter the gap. Also, undesirable melting, indicated by a spherical build up of gold at the gap edge, is discernible by scanning electron microscopy (SEM) in some of the junctions (Figure 1 of Supporting Information).

A necessary condition for successful parallel FCE is obtained by considering the variation in the power dissipated at each junction upon a change in the resistance of the weaker junction, R_{n1}. As R_{n1} increases due to electromigration, the power P_2 dissipated in R_{n2} must increase at a greater rate than P_1 such that

$$\frac{\partial P_1}{\partial R_{n1}} < \frac{\partial P_2}{\partial R_{n1}} \tag{1}$$

When eq 1 is fulfilled, the electromigration naturally balances between the two junctions and they can evolve together. Thus, eq 1 represents an essential stability criterion for parallel electromigration. Returning to the simple case of Figure 1b, the power dissipated by R_{n2} is unaffected by

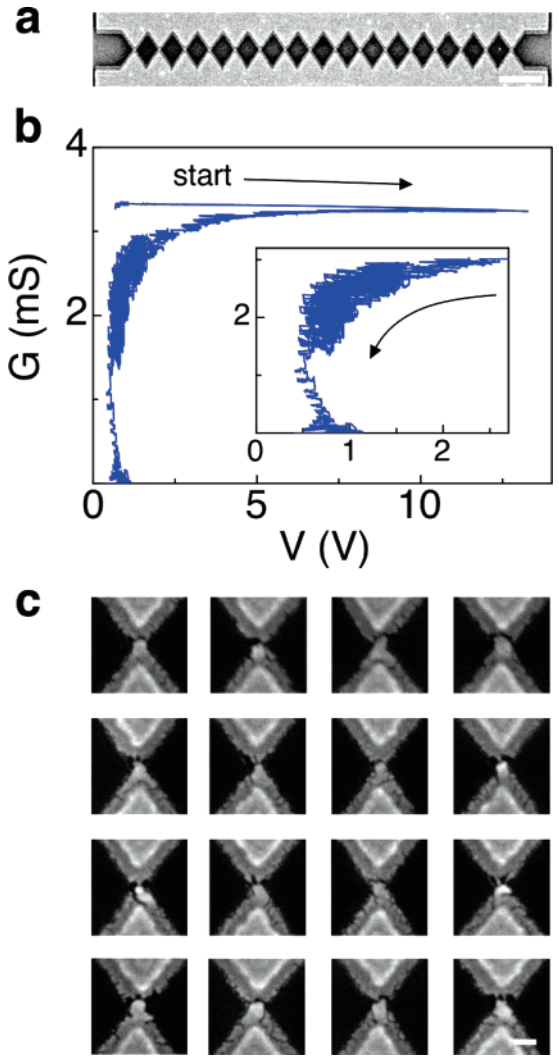

Figure 2. FCE of a 16-junction array. (a) Scanning electron microscope (SEM) image of an array of 16 junctions made by electron beam lithography and shadow evaporation. Scale bar is 1 μm. (b) $G-V$ data from FCE of the 16-junction array. (c) SEM images of nanogaps formed by parallel FCE of a 16-junction array clearly showing the gold removed from the thin overlap junctions. Scale bar is 100 nm.

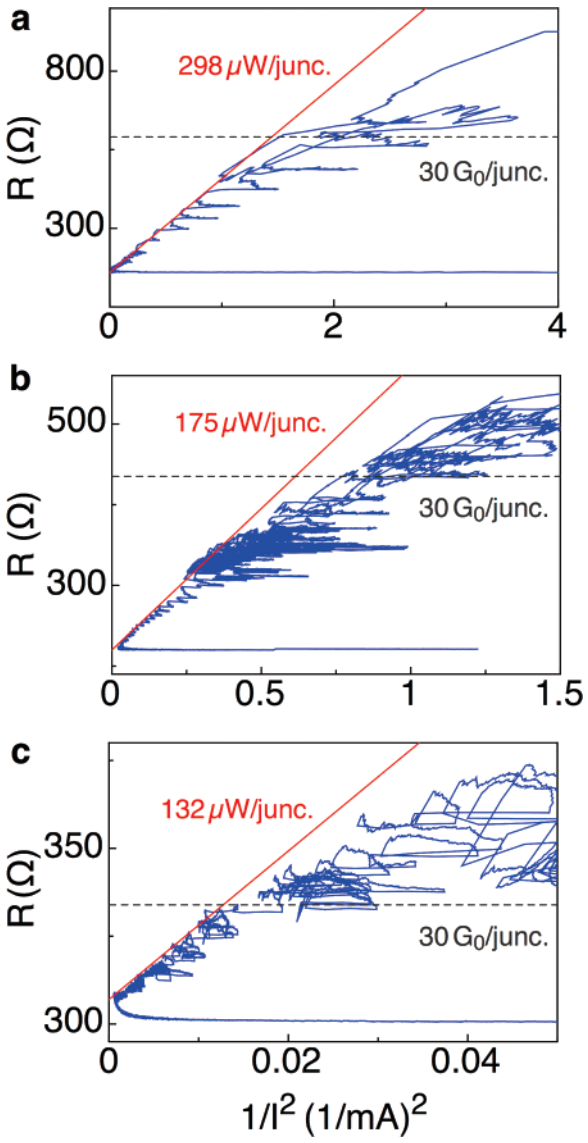

Figure 3. FCE data (blue) from gold junctions undergoing parallel electromigration with linear fit to a critical break power model (red). Deviation from bulk behavior consistently occurs when the sample conductance is reduced below ~30 G_0 per junction. (a) Single junction. (b) Two junctions connected by low interjunction resistance paths. (c) Data from 16-junction array.

changes in R_{n1} when the lead resistance R_L is much larger than both R_{n1} and R_{n2} so that the stability condition is clearly not satisfied.

A circuit design that results in an effective parallel FCE process is presented in Figure 2c. In this case, the junctions share a common series lead resistance R_L and they are connected together by low resistances R_C. As discussed in the Supporting Information, when $R_C < R_{n1},R_{n2}$ the stability condition (eq 1) is satisfied and the nanogaps can evolve together. As the resistance of the weakest junction increases, current is diverted to the other junction and increases its power dissipation and rate of electromigration. This is illustrated by the $G-V$ curve in Figure 1c of a pair of shorted nanogaps electromigrated together. The smooth FCE process is qualitatively indistinguishable from that of a single junction with no evidence of thermal runaway. Parallel FCE of pairs of shorted nanogaps resulted in smooth $G-V$ curves in 3 out of 3 trials.

This process can be extended to the parallel formation of larger arrays of nanogaps, as demonstrated with the 16-junction array pictured in Figure 2a. The $G-V$ curve measured during FCE is shown in Figure 2b. The electromigration process of the array is remarkably similar to that of the single junction (Figure 1a). We find that the time required for the FCE process is essentially the same as for the single junction case, while the measured currents and voltages are scaled up by the number of junctions as expected. Figure 2c shows images of the resulting nanogaps, which are in good agreement with other reports of SEM images of individual nanogaps formed by electromigration.[1,14,15] Although consistent with previous nanogap work, our SEM images do not have sufficient resolution to determine the final distribution of gap sizes. For this reason, the single smooth FCE process of the array is currently the best indication that the

nanogaps evolve in parallel. The future development of arrays compatible with transmission electron microscopy and satisfying the stability condition (eq 1) will enable the direct determination of the nanogap distribution.

Further evidence that this circuit design leads to parallel FCE of the junctions is seen from an analysis of the bulk-neck regime. The bulk-neck regime is characterized by a constant critical power, P^*, dissipated at the junction, which triggers electromigration.[2,4] This implies that $R = R_L + P^*/I^2$, so that a plot of R versus $1/I^2$ should be linear with slope equal to the power dissipation. As shown in Figure 3a, this relationship holds very well when the junction resistance is low, with observable deviations from bulk behavior when the conductance of the junction becomes less than $30G_0$. Remarkably, a similar deviation occurs for the case of two junctions in parallel (Figure 3b) and for 16 junctions (Figure 3c) when the array conductance is less than $30G_0$ per junction. This is indicative of a characteristic change in the nanogap evolution when its conductance falls below $\sim 30G_0$, corresponding to a gold metallic contact with diameter $\sim$1.5 nm or approximately six atoms (here we assume that each atom contributes conductance G_0 and that the atomic radius of gold is 0.14 nm). We also note that the range of critical powers found from the fits in Figure 3 are all within the typical variability of device parameters,[2] although the slight decrease in the critical power per junction with increasing number of junctions in the array may indicate the effect of heating from the other nearby junctions.

Throughout our discussion, we have assumed the use of FCE to fabricate the nanogaps in parallel. One might ask whether it is possible to achieve this goal using this sample design and the single ramp electromigration procedure.[1] Unfortunately, the arrangement engineered with shorts (Figure 1c) is not compatible with the single ramp technique. Because of the resistance R_L, the applied voltage needed to initiate electromigration increases with the number of junctions. As the nanogaps open and their resistances increase during the single ramp procedure, the applied voltage will fall almost completely across the open nanogaps, leading to catastrophic damage and a majority of gap widths greater than 0.5 μm (Figure 2 of Supporting Information).

Nanogap arrays fabricated using this parallel process could be useful for constructing integrated circuits of molecular-scale electronics. Progress toward this goal will require the development of techniques for removing the metallic shorts connecting the nanogaps once they have been formed, which will also enable the determination of the final distribution of nanogap sizes through electrical measurements. One possibility is to incorporate sacrificial shorts that are selectively etched away once the nanogaps are formed. For other particular applications (e.g., to use the nanogaps to measure surface-enhanced Raman spectroscopy of molecules[16]), the nanogaps could be left shorted together.

In summary, we have developed a reproducible and controllable parallel process for creating electromigrated nanogaps in metal electrodes. The process relies on feedback-controlled electromigration to fabricate nanogaps in an array of shorted gold junctions. Parallel electromigration of nanogaps is achieved when the interjunction resistance is smaller than the individual junction resistance. We demonstrated the controlled parallel formation of 16 nanogaps in an array of gold junctions and have developed a methodology for scaling this up to large-scale circuits.

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Supporting Information Available: Details of the sample fabrication, the mathematical details of the circuit design considerations for parallel electromigration, and data from sequential and single ramp electromigration arrays. This material is available free of charge via the Internet at http://pubs.acs.org.

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